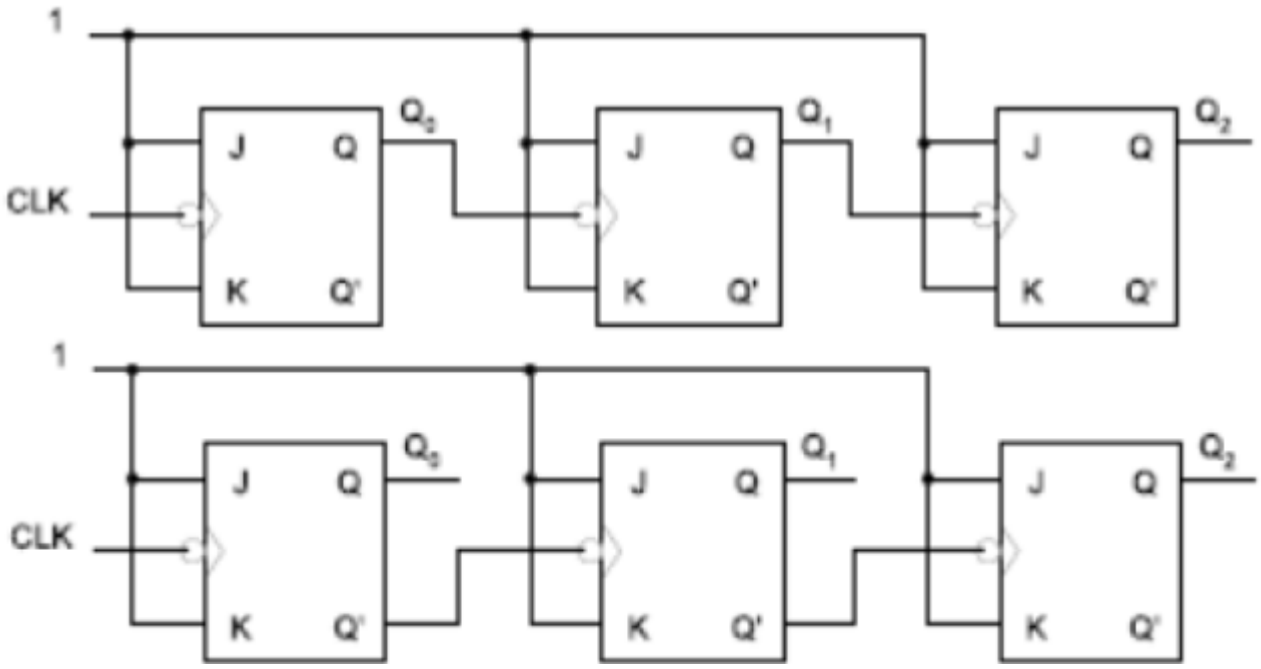
Logic Lab – Exp #10 30.04.2019

Asynchronous Counters

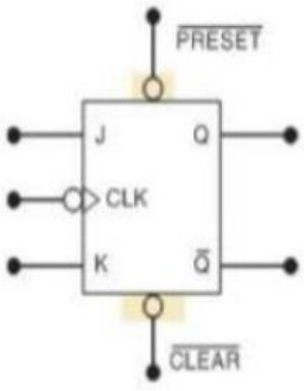
Y-0016/004D and 0001/2D board (given in next page)

In the 3-bit counters given below, negative (falling) edge triggered flip-flops have been used. (This is indicated by the small circle in front of the clock input.)

1. Draw the timing diagrams accordingly.



2. Design a **Mod-5** asynchronous counter. A Mod-5 counter counts **0-1-2-3-4-0**. First determine the number of flip-flops, and for an up counter. Then, form the resetting mechanism for the output of 6. You can use the CLEAR input of the flip-flops. Construct the circuit, and check your results.



- $\overline{\text{PRESET}} = \overline{\text{CLEAR}} = 1$. The asynchronous inputs are inactive and the FF is free to respond to the *J*, *K*, and *CLK* inputs; in other words, the clocked operation can take place.
- $\overline{\text{PRESET}} = 0$; $\overline{\text{CLEAR}} = 1$. The $\overline{\text{PRESET}}$ is activated and *Q* is *immediately* set to 1 no matter what conditions are present at the *J*, *K*, and *CLK* inputs. The *CLK* input cannot affect the FF while $\overline{\text{PRESET}} = 0$.
- $\overline{\text{PRESET}} = 1$; $\overline{\text{CLEAR}} = 0$. The $\overline{\text{CLEAR}}$ is activated and *Q* is *immediately* cleared to 0 independent of the conditions on the *J*, *K*, or *CLK* inputs. The *CLK* input has no effect while $\overline{\text{CLEAR}} = 0$.
- $\overline{\text{PRESET}} = \overline{\text{CLEAR}} = 0$. This condition should not be used because it can result in an ambiguous response.