Logic Lab – Exp #7

Sequential Logic Gates

Y-0016/003D and Y-0016/001D

1. Fill in the characteristic table for **SR Latch** and **SR Flip-flop** using **Y-0016/003D** board**.**

2. Verify the characteristic table of **D flip-flop** using **Y-0016/003D** board**.**

3. Create an equivalent circuit of the **JK flip-flop** using a single **D flip-flop** and verify characteristic table of **JK flip-flop.**

4. Create an equivalent circuit of the **T flip-flop**, using a single **D flip-flop** and verify characteristic table of **T flip-flop.**

5. Verify the characteristic table of **JK flip-flop** using **JK flip-flop** on **Y-0016/003D** board**.**

***D* Flip-Flop**

D	*Q*(*t* + 1)	
0	0	Reset
1	1	Set

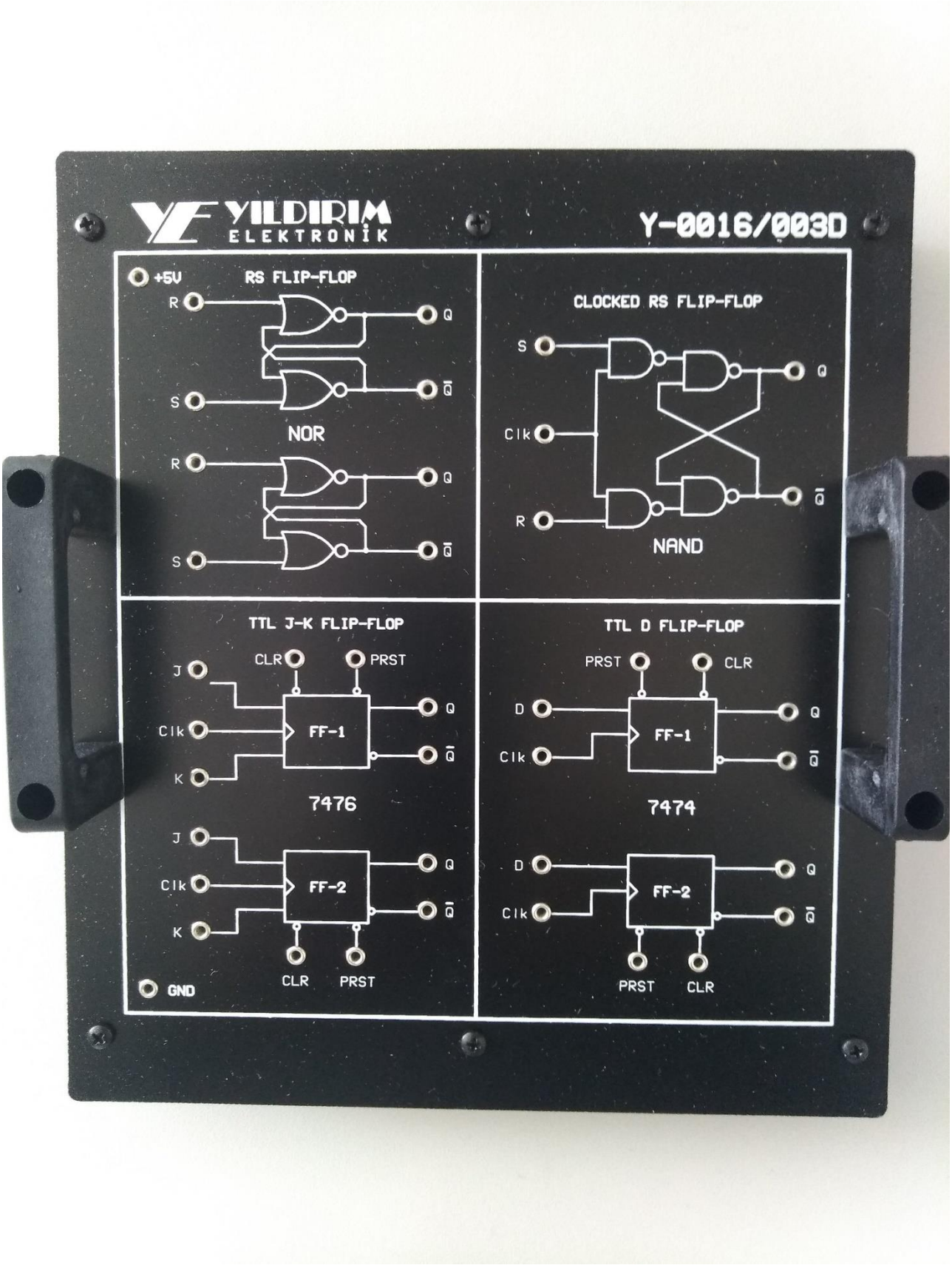
***JK* Flip-Flop**

J	*K*	*Q*(*t* + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

***T* Flip-Flop**

T	*Q*(*t* + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

Logic Lab – Exp #7



Logic Lab – Exp #7