Logic Lab – Exp #8 **09.04.2019**

Sequential Circuit Synthesis

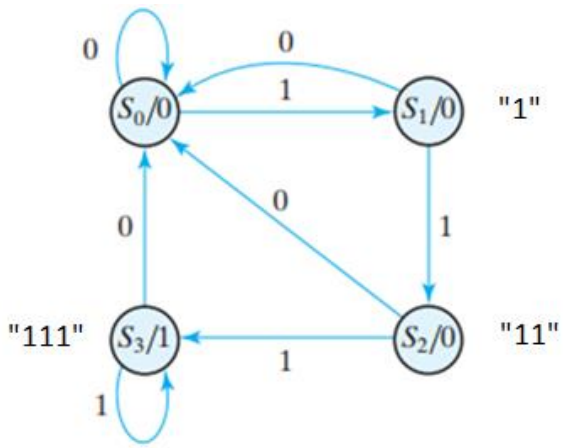
Y-0016/004D and 001/2D board (given in next page)

Verfiy JK flip flops with the truth table using Y-0016/004D board for each FF.

Design Example

Suppose we wish to design a circuit that detects a sequence of three or more consecutive 1's in a string of bits coming through an input line. The input is a serial bit stream.

State diagram



Present State		Input	Next State		Output
A	*B*	*x*	*A*	*B*	*y*
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

Using JK flipflop and its excitation table:

Q(*t*)	*Q*(*t* + 1)	*J*	*K*
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(a) *JK* Flip-Flop

State Table and JK Flip-Flop Inputs

Present State		Input	Next State		Flip-Flop Inputs			
A	*B*	*x*	*A*	*B*	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	0	0	0	X	X	1
0	1	1	1	0	1	X	X	1
1	0	0	0	0	X	1	0	X
1	0	1	1	1	X	0	1	X
1	1	0	0	0	X	1	X	1
1	1	1	1	1	X	0	X	0

After filling J, K in the table, Karnough map will be used to simplfy and to find inputs of JK flipflops.

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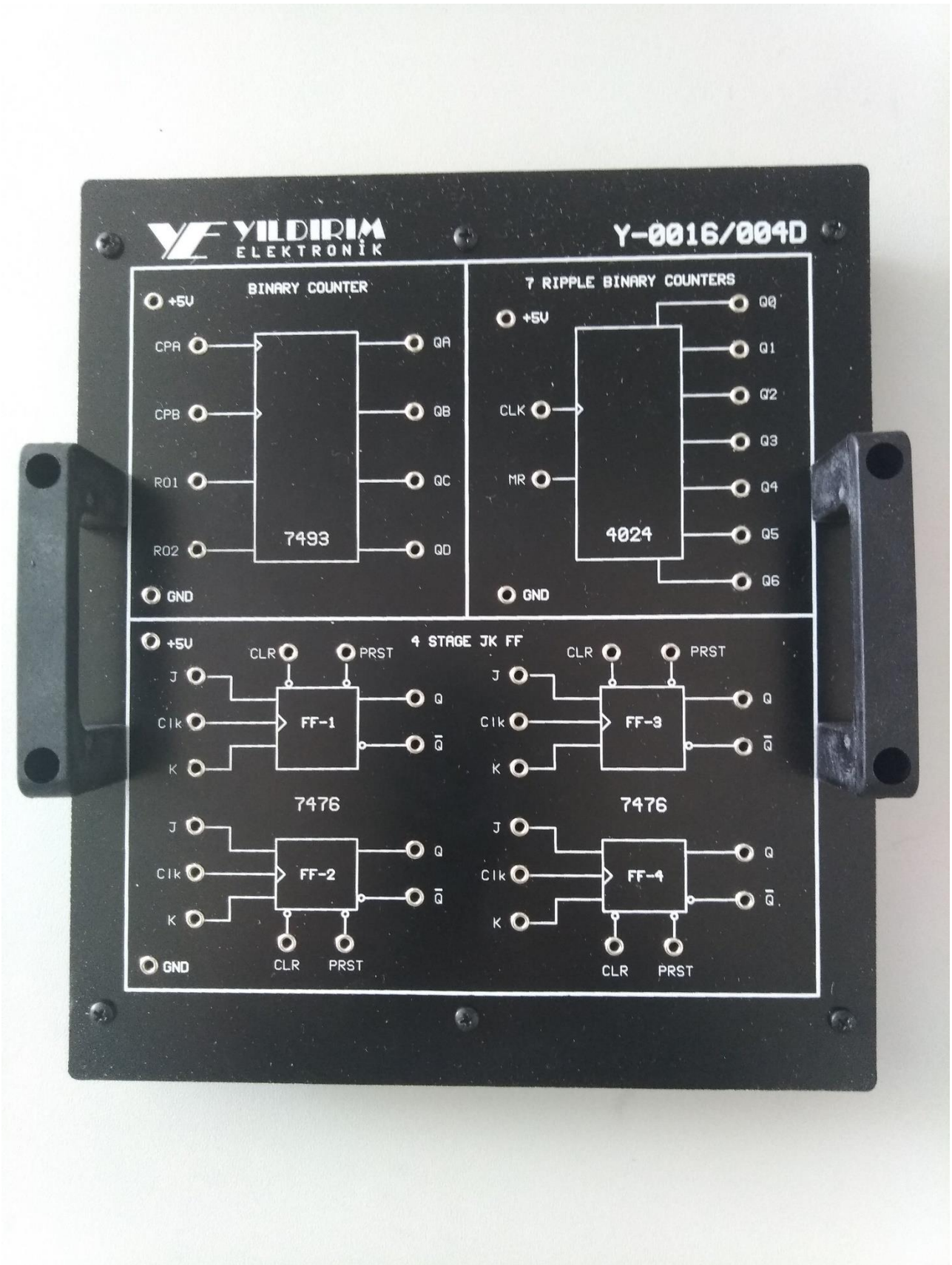
1. A stream of **0's** and **1's** coming from a serial transmission channel. A sequential circuit will be designed that detects 011 sequence coming through this input line.

   a. Draw the state diagram.
   b. Fill in the state table using JK flipflops
   c. Simplify the JKs in Karnough and find their input definitions
   d. Implement the circuit using Y-0016/004D board and other necessary gate boards.


YILDIRIM
ELEKTRONİK
Y-0016/004D
BINARY COUNTER
+5V
CPA
CPB
R01
R02
7493
QA
QB
QC
QD
GND
7 RIPPLE BINARY COUNTERS
+5V
CLK
MR
4024
Q0
Q1
Q2
Q3
Q4
Q5
Q6
GND
4 STAGE JK FF
+5V
CLR
PRST
J
Clk
K
FF-1
Q
Q̄
FF-3
7476
FF-2
FF-4
GND