Logic Lab – Exp #3

Gate Level Minimization and Combinational Circuit Synthesis

Y-0016/002D boards (given in the last page)

1) a) Simplify the given function ***F*** using **Karnough map** and don't care condition.

$$F(A, B, C, D) = \sum (0,1,3,5,8,9,10,13)$$
$$\text{Don't Care Cond} = \sum (2)$$

b) Draw and implement the minimized function using **Y-0016/002D** board.

c) Fill in the truth table using the inputs and output on the experiment set and verify results with original function ***F***.

Logic Lab – Exp #3

2) a) Simplify the given function ***F*** using **Quine Mc Cluskey tabular method** and don't care condition.

$$F(A, B, C, D) = \sum (9,10,11,13,14,15)$$
$$\text{Don't Care Cond} = \sum (2,6)$$

b) Draw and implement the minimized function using **Y-0016/002D** board.

c) Fill in the truth table using the inputs and output on the experiment set and verify results with original function ***F***.

Logic Lab – Exp #3