EXPERIMENT 7.3

EXAMINATION OF JFET'S INPUT CHARACTERISTICS

EXPERIMENTAL PROCEDURE:

Plug the Y-0016/012 module. Make the circuit connections as in Figure 7.5.

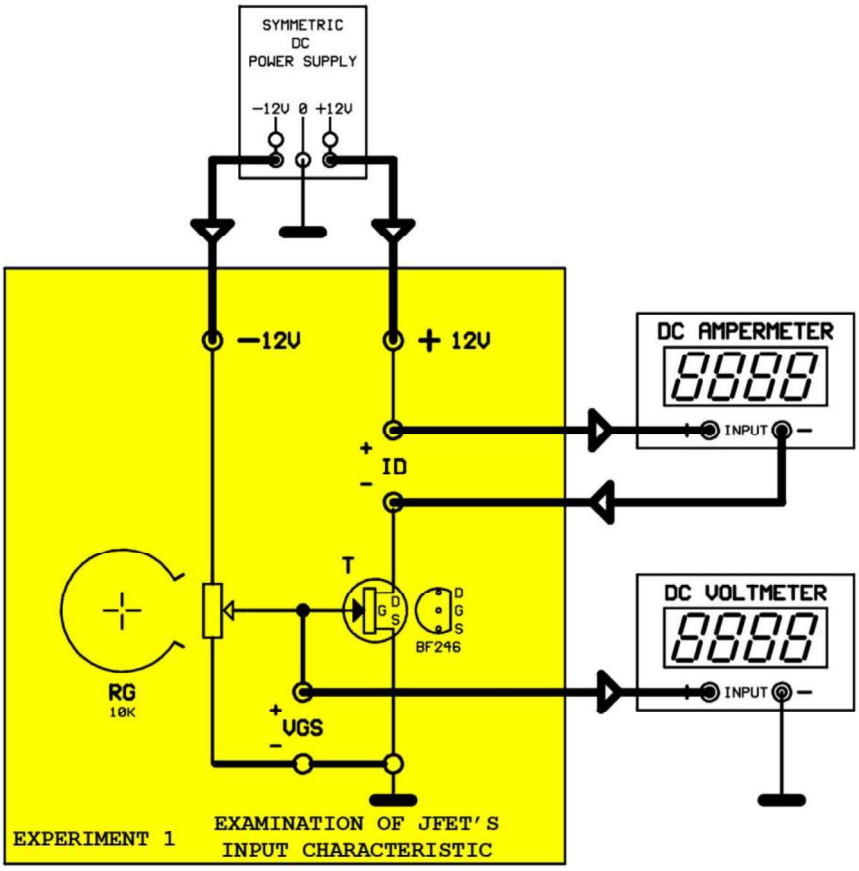

Figure 7.5

1- Type the VGS voltage to the table at Figure 7.6 with the help of RG potentiometer. Also type the ID values for each step.

V_{DS}=12V CONSTANT	
V_{GS} (VOLT)	I_D (mA)
0.0	
-0.5	
-1.0	
-1.5	
-2.0	
-2.5	
-3.0	
-3.5	
-4.0	

Figure *7.6*

2- Draw the VGS/ID curve using the values in Figure 7.6.

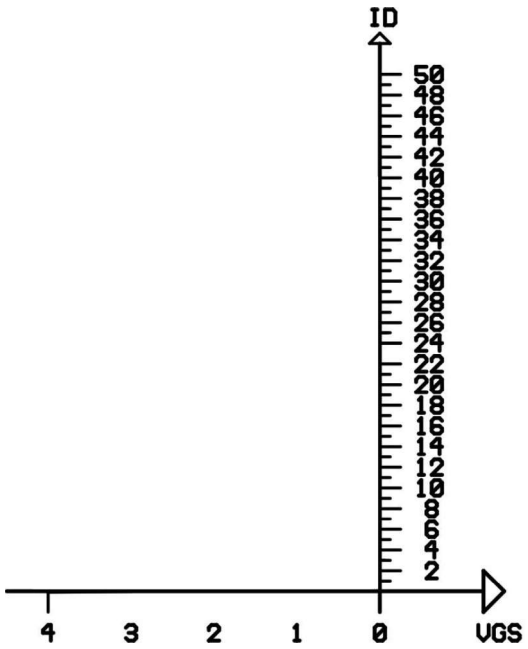

Figure 7.7

3- When the **VGS=**-3.5V or at a smaller value **ID=**"**0**". What is the name for this value of VGS?

EXPERIMENT: 7.4

EXAMINATION OF JFET'S OUTPUT CHARCTERISTICS

EXPERIMENTAL PROCEDURE:

Plug the Y-0016/012 module. Before making the connections, adjust the output voltage of power supply to "**0**" by rotating voltage potentiometers to left. And adjust the gate voltage to "**0**" by rotating the "**RG**" potentiometer to left.

Make the circuit connections as in Figure 7.8 and apply energy to circuit.

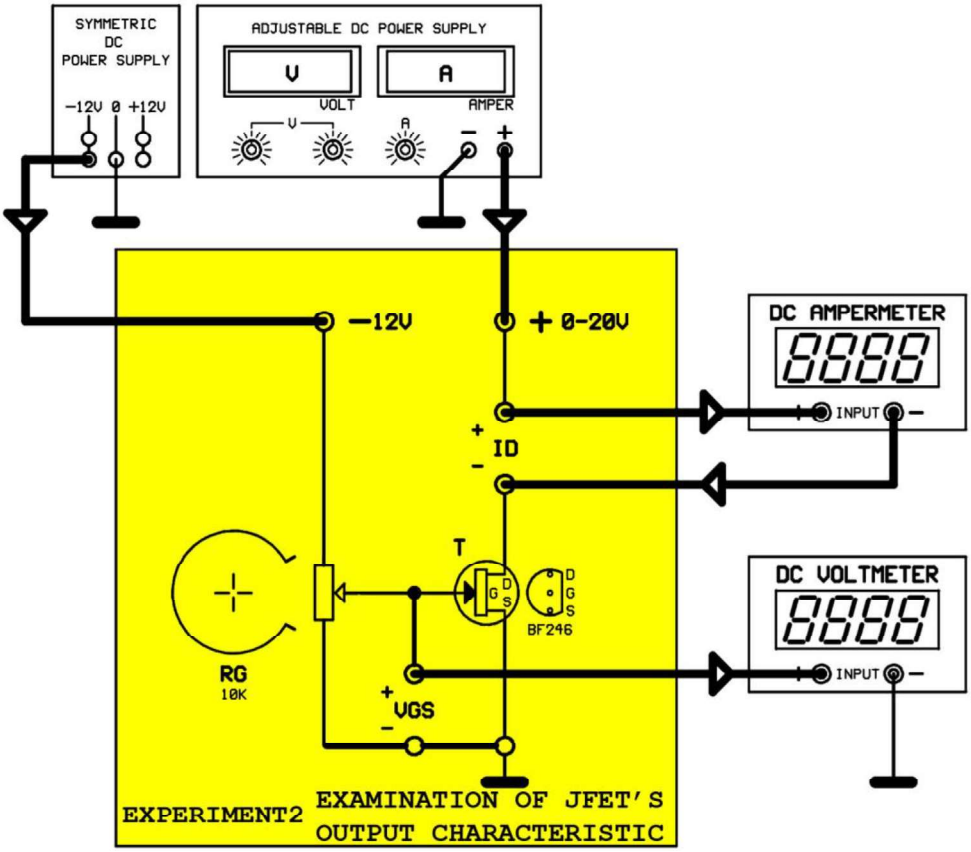

Figure 7.8

1- Set **VGS**=0 using "**RG**" potentiometer. Adjust the power supply voltage to the VDS voltage values in Figure 7.9 and make sure that **VGS=0** at each step. Type the ID values at each step to section "**A**".

VGS=0 CONSTANT	
VDS (VOLT)	ID (mA)
1	
2	
3	
4	
5	
10	
15	
20	

A

VGS=-1 CONSTANT	
VDS (VOLT)	ID (mA)
1	
2	
3	
4	
5	
10	
15	
20	

B

VGS=-2 CONSTANT	
VDS (VOLT)	ID (mA)
1	
2	
3	
4	
5	
10	
15	
20	

C

VGS=-3 CONSTANT	
VDS (VOLT)	ID (mA)
1	
2	
3	
4	
5	
10	
15	
20	

D

VGS=-4 CONSTANT	
VDS (VOLT)	ID (mA)
1	
2	
3	
4	
5	
10	
15	
20	

E

Figure 7.9

2- Draw the change graphic between VDS/ID axes like in Figure 7.10

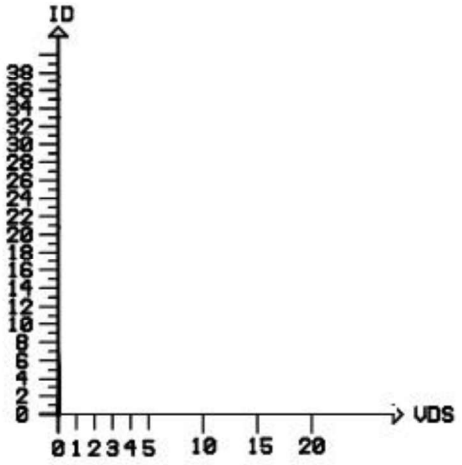

Figure 7.10

3- ID is constant even if the VDS is increased. What is the name for this value of ID?

4- Adjust the VGS voltage to–1V, -2V, -3V, -4V, respectively. Adjust the VDS voltage to the values in Figure 7.11 and type each ID value next to each VDS value.

VGS=0 CONSTANT	
VDS (VOLT)	ID (mA)
1	
2	
3	
4	
5	
10	
15	
20	

A

VGS=-1 CONSTANT	
VDS (VOLT)	ID (mA)
1	
2	
3	
4	
5	
10	
15	
20	

B

VGS=-2 CONSTANT	
VDS (VOLT)	ID (mA)
1	
2	
3	
4	
5	
10	
15	
20	

C

VGS=-3 CONSTANT	
VDS (VOLT)	ID (mA)
1	
2	
3	
4	
5	
10	
15	
20	

D

VGS=-4 CONSTANT	
VDS (VOLT)	ID (mA)
1	
2	
3	
4	
5	
10	
15	
20	

E

Figure 7.11

5- Draw change graphics between VDS/ID axes for each VGS voltage value like in Figure 7.10.

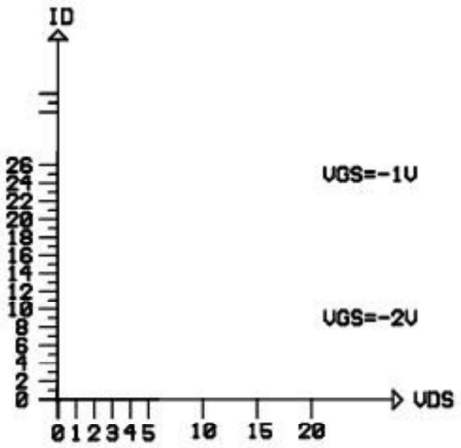

Figure 7.12

6- What is the name for these graphics?

7- Write the effect of gate bias to drain current.

8- Write the effect of VDS voltage to drain current.