Questions

1. Design an adder that adds 4 2-bit numbers. Clearly define the operations and bit lengths. You are not allowed to use any pre-defined primitives (e.g. Full Adder).

2. Design a multiplier that multiplies 3 2-bit numbers. Clearly define the operations and bit lengths. You are not allowed to use any pre-defined primitives.

3. Assume you are living on a planet, where a day is 5 hours, an hour is 10 minutes and a minute is 10 seconds. Design a digital clock that will work on this planet.

4. Design a machine that outputs a 1 when exactly two of the last three inputs are 1.

5. Consider the sequential circuit below. Assume that, by using the signal P, the flip flops are brought to the initial state $Q_3 = 0, Q_2 = 1, Q_1 = 1, Q_0 = 0$.

6. Design a simple datapath for the register transfer shown by the pseudo-code below, where X, Y, Z, W are four registers, and C1 and C2 are two control signals coming from the controller. Use a 4-to-1 multiplexer with select signals S1 and S0. Assume the registers Y, Z, and W are connected to the 00, 01, and 10 input lines, respectively, of the multiplexer.

- Fill the table below (where CLK1 is the first rising edge of the clock, CLK2 is the second rising edge of the clock, and so on) until the states start repeating.

<table>
<thead>
<tr>
<th></th>
<th>$Q_3$</th>
<th>$Q_2$</th>
<th>$Q_1$</th>
<th>$Q_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK1</td>
<td></td>
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<tr>
<td>CLK2</td>
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<tr>
<td>CLK3</td>
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<td>CLK4</td>
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<td>CLK5</td>
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<tr>
<td>CLK6</td>
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</tr>
</tbody>
</table>

- Draw the state transition diagram of this circuit.

6. Design a simple datapath for the register transfer shown by the pseudo-code below, where X, Y, Z, W are four registers, and C1 and C2 are two control signals coming from the controller. Use a 4-to-1 multiplexer with select signals S1 and S0. Assume the registers Y, Z, and W are connected to the 00, 01, and 10 input lines, respectively, of the multiplexer.
if \( (C1 == 1) \)
\[
X = Y
\]
else if \( (C2 == 1) \)
\[
X = Z
\]
else
\[
X = W
\]

Draw the datapath, showing the registers, the multiplexer, all the connections, and the multiplexer select signals. Derive the Boolean equations of the select signals \( S_1 \) and \( S_0 \) in terms of the control signals \( C1 \) and \( C2 \).

7. You are asked to design an even parity checker, which is a sequential circuit that has one input \( (X) \) and one output \( (Z) \). The output is \( Z = 1 \) if and only if the total number of 1s received is even (for example, 0, 2, 4, 6, ... ), \( Z = 0 \) otherwise.

8. Consider the following Boolean function,
\[
F = \overline{AB}C + ABC + AB\overline{D} + A\overline{B}D + \overline{A}B\overline{C}D + \overline{A}BCD + \overline{A}\overline{B}CD
\]

The function \( F \) is implemented by the following circuit.

\( F_0, F_1, F_2, F_3 \) are combinational circuits with inputs \( X, Y \). For the multiplexer select signals, \( S_1 \) is the MSB and \( S_0 \) is the LSB. For (I) through (IV), circle the function that you would use to implement \( F_0 \) to \( F_3 \). Use the following choices to answer each question.

(a) \( Z = X \oplus Y \)
(b) \( Z = \overline{(XY)} \)
(c) \( Z = \overline{X} \oplus \overline{Z} \)
(d) $Z = X + Y$
(e) $Z = XY$
(f) $Z = (X + Y)$

(I) $F_0$ should be: (a) (b) (c) (d) (e) (f)
(II) $F_1$ should be: (a) (b) (c) (d) (e) (f)
(III) $F_2$ should be: (a) (b) (c) (d) (e) (f)
(IV) $F_3$ should be: (a) (b) (c) (d) (e) (f)